Integrative Optimization of Functional Testing Machines

1 Introduction

Welcome to the 2026 Industry Sprint Workshop (ISW) at the International DSM Conference. ISW have a year-long tradition at DSM conferences, and we are happy to continue this format.

We are delighted to present **ABB** as our industry partner for this year's challenge. We will work on an exciting task to analyze and derive recommended improvements for ABB's **Functional Testing Machines (FTM)**, where current adaptions to new microcontrollers as tested objects are taking too much time. We will investigate the three domains of product, process, and organization, to be able to derive insights on the **integration** of those three domains.

You will have **~ 2,5 h time** to **solve the task** and **prepare** a small **presentation** of **max. 5 min**. A jury will evaluate your presentations and define a winning team, awarded with a small prize. Additionally, each group will get a 30 min guided lab tour visiting the FTMs.

Below, Figure 1 gives you an overview of today's ISW schedule:

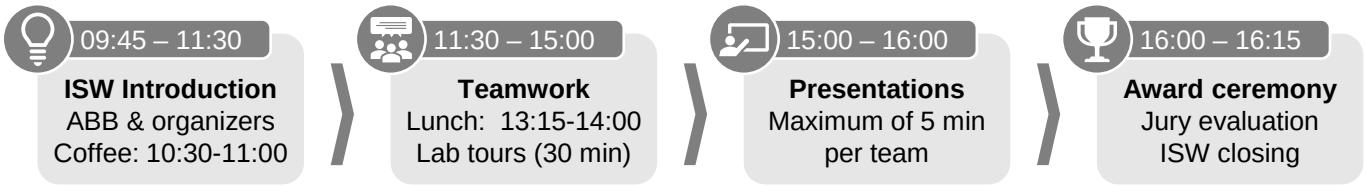

Figure 1: Industry Sprint Workshop (ISW) schedule

2 Background

An end-of-line testing machine (FTM) verifies the quality of the production process, ensuring that each **electronic board** has been correctly manufactured and meets the required functional and accuracy requirements.

The change concerns the replacement of the **main microcontroller with a new MCU-X part in the electronic boards to be tested**. It is reported by **Supply Chain Management (SCM) & Product Engineering**, triggering the **Product Owner** to issue an **Engineering Change Notice (ECN).** Although the new MCU is considered "functionally compatible" (minimal impact on the FTM design) **the actual impact found by Test Engineering can be much larger** than expected due to three types of dependencies:

- **FTM dependencies (Product DSM):** the new MCU may affect other FTM elements; e.g., the test bench fixture (nest + pogo pins).
- **Process dependencies (Process DSM):** issues may propagate across activities; e.g., electrical design problems discovered only during validation can trigger late redesign.
- **Organizational dependencies (Organization DSM):** the change requires coordination between Test Engineering and the external FTM supplier's Firmware, HW, and Fixture teams.

Identifying these dependencies is key to understanding the real impact of the change and reducing the FTM update lead time, currently estimated at almost 25 weeks.

3 What we ask of you

- Review and discuss the available data/models. Understand all three domains and discuss if anything is missing that you might consider important.
- Review the pre-analyzed change impact reports of the microcontroller. Understand what impact a change in this part causes in the whole multi-domain system and identify which elements are impacted the most. Briefly discuss possible reasons (but focus on next steps)
- Review each domain and suggest possible improvements in each domain separately. Include the pre-analyzed DSM views into your considerations
- Discuss the integration of the three domains: consider dependencies between domains and suggest changes for the overall system
- Prepare a presentation of max. 5 min. At least discuss each domain and the integration view. Also include a traceability from your decisions back to the given models as far as possible
- A more detailed description of the tasks is provided in **Section 7, Guideline**.

Our partners from Lattix are here to support you. All the models shown in the following are available as models in Lattix on the machines of the Lattix representatives. If you want to investigate a certain change you consider, you can consult them to directly view the models.

4 Detailed description of the Functional Testing Machines (FTM)

The following figures describe the product domain separately with its three dependency kinds, and then the mutli-domain view with all three domains.

Product-DSM (Figures 2, 3, 4, 5)

Code	Product*
E1	Microcontroller (MCU-X)
E2	Programming connector
E3	Existing test points (incl. TP3 – clock)
E4	New test points (TP9, TP10)
E5	DUT firmware
E6	PCB layout/pinout – DUT board, MCU area
E7	EOL test bench adapter electrical layout
E8	EOL test bench fixture (nest + pogo pins)
E9	EOL test firmware
E10	FTM software
E11	Technical documentation

* note: the elements from E1 to E5 are part of the Device Under Testing (DUT, the electronic board) and therefore are the initiators of the changes **but are out of scope for the redesign of the FTM** (which instead should include the elements from E6 to E11).

Part of the FTM architecture, focus for the redesign in the workshop

DSM convention: Cell (i, j) shows how strongly the row element i **depends on** the column element j – if j changes, i must be reviewed or modified (1 = weak/indirect, 2 =moderate, 3 = strong/direct).

Color legend: Green: mechanical interface, Pink: electrical interface, Blue: information interface. When a cell has multiple colors it means the interfaces are multiple (e.g. a green and pink cell = both mechanical and electrical interface)

Process-DSM (MDM in Figure 6)

Code	Process activity	Duration (weeks)
P1	Requirements / specifications receipt	1
P2	Test strategy definition	1
P3	Electrical design of test machine / fixture	3
P4	Mechanical fixture design	3
P5	Component procurement*	
P6	Test machine / fixture manufacturing	4
P7	Test firmware development	3
P8	Test sequence development	2
P9	Assembly	2
P10	HW–SW integration	2
P11	Internal validation	3
P12	Factory Acceptance Test (FAT)	1
	Total nominal process duration	**25**

*Note: Component procurement is carried out **concurrently** with electrical and mechanical fixture design

DSM convention: Cell (i, j) represents how strongly the process on the row **depends on** the output of process in the column: 1 = weak (informational, low risk), 2 = moderate (functional, requires coordination), 3 = strong (structural/physical, constraining). Cells over the diagonal indicate **feedback loops.**

Organization-DSM (MDM in Figure 6)

Code	Organizational actor / role
B1	SCM & Product Engineering
B2	Product Owner
B3	R&D – HW Designer
B4	R&D – Electronic Layout
B5	R&D – FW Designer
B6	Test Engineering
B7	FTM Supplier – Firmware & Test Sequence
B8	FTM Supplier – Test Machine Hardware
B9	FTM Supplier – Mechanical Fixture

DSM convention: Cell (i, j) represents how strongly actor on the row **depends on** the output of the actor in the column (i → j): 0 = none, 1 = weak/informal, 2 = moderate/formal, 3 = strong/critical (blocking).

Start DSM - Default Filters			E1: Microcontroller (MCU-X) 1	E2: Programming connector 2	E3:Existing test points (incl. TP3 - clock) 3	E4: New test points (TP9, TP10) 4	E5: DUT firmware 5	E6: PCB layout/pinout - DUT board, MCU area 6	E7: EOL test bench adapter electrical layout 7	E8: EOL test bench fixture (nest ...nufacturer 8	E9: EOL test firmware 9	E10: FTM software 10	E11: Technical documentation 11	PROCESS 12	ORG 13
PRODUCT	DUT	E1: Microcontroller (MCU-X) 1	.					3		2				7	6
		E2: Programming connector 2	1	.				2	3	3				10	6
		E3:Existing test points (incl. TP3 - clock) 3	3		.	1		2	2					11	4
		E4: New test points (TP9, TP10) 4	3			.		3						12	6
		E5: DUT firmware 5	3		1	1	.							7	5
	E6: PCB layout/pinout - DUT board, MCU area 6		4	3		2		.	2	3				10	6
	E7: EOL test bench adapter electrical layout 7			4		3		3	.	3				9	3
	E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer 8		2	4	1	4		3	4	.				9	3
	E9: EOL test firmware 9		2		3	2	3				.			6	3
	E10: FTM software 10					2	1				2	.		5	2
	E11: Technical documentation 11		2	1	1	2	1	2	1	2	1	1	.	12	9
PROCESS 12														.	50
ORG 13															.

Figure 2: FTMs product domain with all dependencies – initial structure

Mechanical - Mechanical			1	2	3	4	5	6	7	8	9	10	11	12	13
PRODUCT	DUT	E1: Microcontroller (MCU-X) 1	.					3		2					
		E2: Programming connector 2		.				2	3	3					
		E3:Existing test points (incl. TP3 - clock) 3			.	1		2	2						
		E4: New test points (TP9, TP10) 4				.		3							
		E5: DUT firmware 5			1		.								
	E6: PCB layout/pinout - DUT board, MCU area 6		3	2				.	2	3					
	E7: EOL test bench adapter electrical layout 7			3				2	.	3					
	E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer 8		2	3		3		3	3	.					
	E9: EOL test firmware 9				2						.				
	E10: FTM software 10											.			
	E11: Technical documentation 11												.		
PROCESS 12														.	
ORG 13															.

Figure 3: FTMs product domain with mechanical dependencies only – initial structure

Energy - Energy	E1: Microcontroller (MCU-X) 1	E2: Programming connector 2	E3:Existing test points (incl. TP3 - clock) 3	E4: New test points (TP9, TP10) 4	E5: DUT firmware 5	E6: PCB layo...pinout - DUT board, MCU area 6	E7: EOL test bench adapter electrical layout 7	E8: EOL test bench fixture (nest ...nufacturer 8	E9: EOL test firmware 9	E10: FTM software 10	E11: Technical documentation 11	PROCESS 12	ORG 13
PRODUCT / DUT / E1: Microcontroller (MCU-X) 1	.												
PRODUCT / DUT / E2: Programming connector 2	1	.											
PRODUCT / DUT / E3:Existing test points (incl. TP3 - clock) 3	3		.										
PRODUCT / DUT / E4: New test points (TP9, TP10) 4	3			.									
PRODUCT / DUT / E5: DUT firmware 5					.								
PRODUCT / E6: PCB layout/pinout - DUT board, MCU area 6	1	1				.							
PRODUCT / E7: EOL test bench adapter electrical layout 7		1		3		1	.						
PRODUCT / E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer 8		1	1	1			1	.					
PRODUCT / E9: EOL test firmware 9			1						.				
PRODUCT / E10: FTM software 10										.			
PRODUCT / E11: Technical documentation 11											.		
PROCESS 12												.	
ORG 13													.

Figure 4: FTMs product domain with energy dependencies only – initial structure

Information - Information	E1: Microcontroller (MCU-X) 1	E2: Programming connector 2	E3:Existing test points (incl. TP3 - clock) 3	E4: New test points (TP9, TP10) 4	E5: DUT firmware 5	E6: PCB layout/pinout - DUT board, MCU area 6	E7: EOL test bench adapter electrical layout 7	E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer 8	E9: EOL test firmware 9	E10: FTM software 10	E11: Technical documentation 11	PROCESS 12	ORG 13
PRODUCT / DUT / E1: Microcontroller (MCU-X) 1	.												
PRODUCT / DUT / E2: Programming connector 2		.											
PRODUCT / DUT / E3:Existing test points (incl. TP3 - clock) 3			.										
PRODUCT / DUT / E4: New test points (TP9, TP10) 4				.									
PRODUCT / DUT / E5: DUT firmware 5	3			1	.								
PRODUCT / E6: PCB layout/pinout - DUT board, MCU area 6				2		.							
PRODUCT / E7: EOL test bench adapter electrical layout 7							.						
PRODUCT / E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer 8								.					
PRODUCT / E9: EOL test firmware 9	2			2	3				.				
PRODUCT / E10: FTM software 10				2	1				2	.			
PRODUCT / E11: Technical documentation 11	2	1	1	2	1	2	1	2	1	1	.		
PROCESS 12												.	
ORG 13													.

Figure 5: FTMs product domain with information dependencies only – initial structure

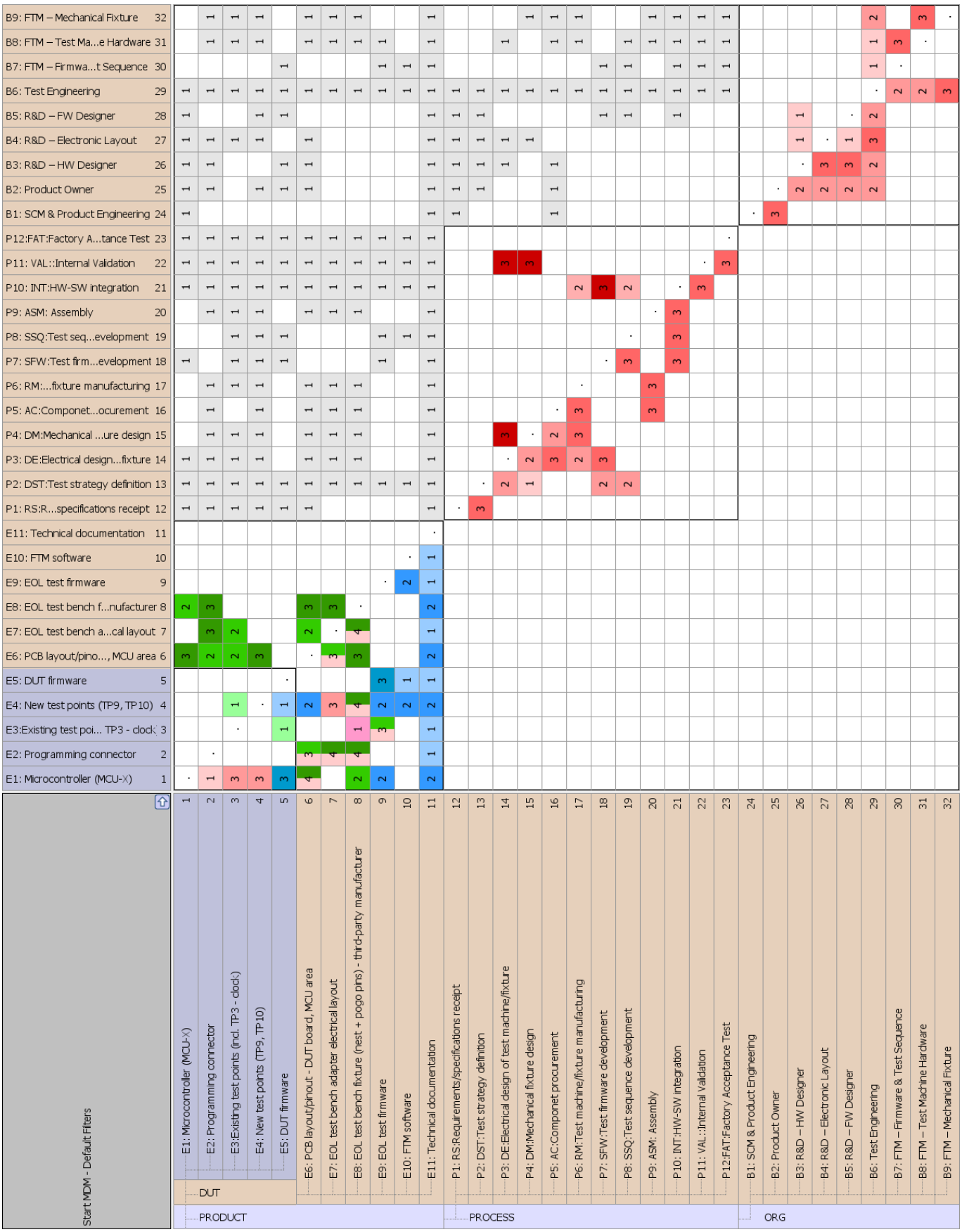

Figure 6: FTMs multi-domain view with product, process and org domain and related dependencies between them – initial structure

5 Pre-analyzed models

To support your analysis, we have pre-analyzed the three domains in a first step. The product and organization domain have been clustered, and the process domain has been sequenced.

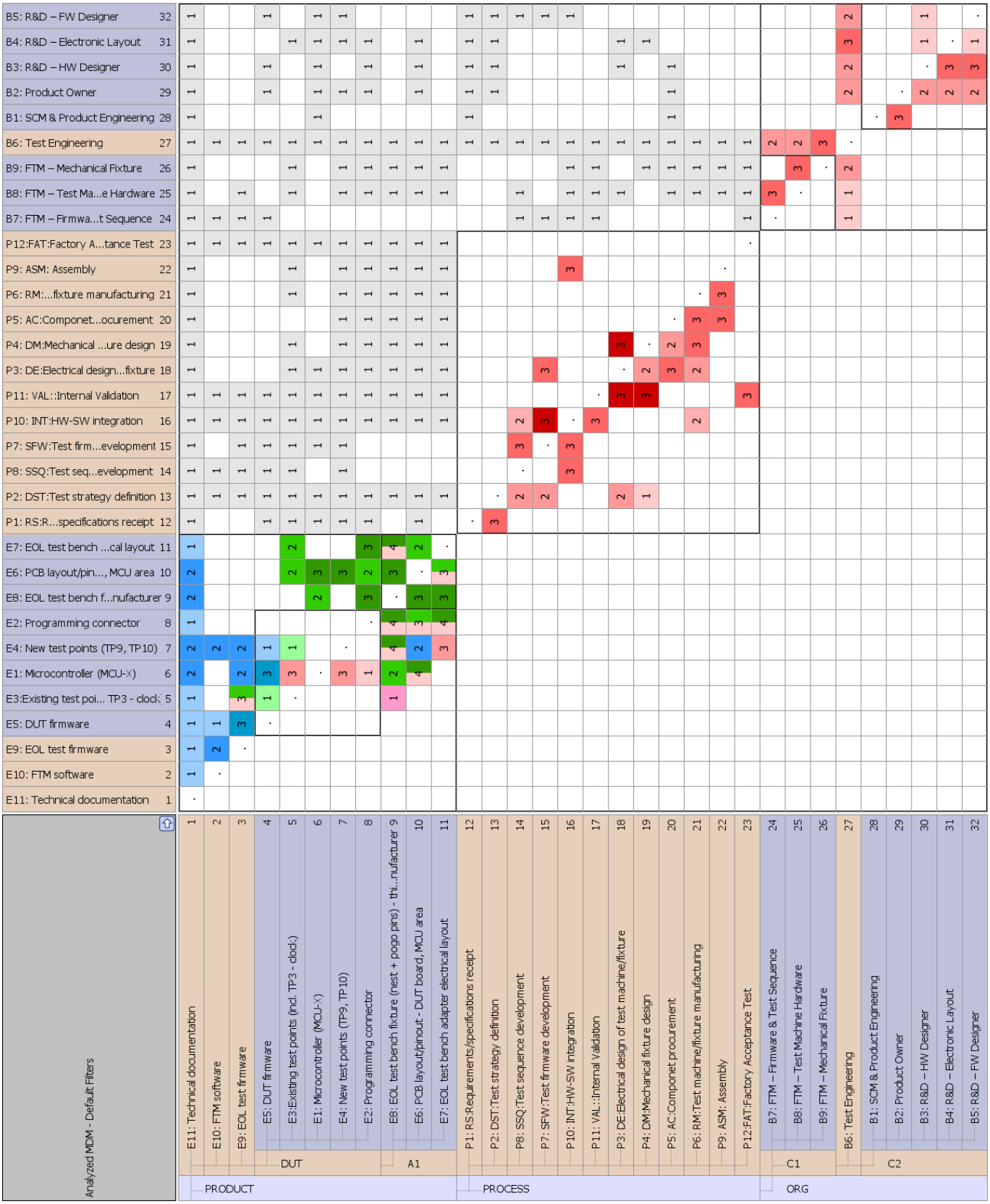

Figure 7: FTMs multi-domain view with product, process and org domain and related dependencies between them – pre-analyzed structure

6 Change impact analysis for the microcontroller

To further support your analysis, we have used the change impact report function of Lattix. It presents you lists of direct dependencies (level 1) and indirect dependencies (level 2) affected by the microcontroller. It is split into “impacts”, i.e., which dependencies from the microcontroller exist to another element (Tables 1 and 2), and “uses”, i.e., which elements the microcontroller depends on (Tables 3 and 4).

For the important dependencies identified and discussed by you, **you should also use your intuition to identify the reason behind the relationship and its strength (weight).** For example, following **one possible propagation path**:

Microcontroller → PCB layout → EOL test bench

At Level 1, the microcontroller directly impacts the PCB layout (weight = 3) **because** the new MCU package requires a different footprint/land pattern in the MCU area.

At Level 2, this change indirectly impacts the EOL test bench (weight = 3) **because** the PCB layout determines the exact XY coordinates of the probes in the test nest. A change initially affecting the microcontroller can therefore propagate to an element that has no direct dependency on the microcontroller itself.

Use the same reasoning to interpret the other Level 1 and Level 2 dependencies reported by Lattix and reconstruct the possible causal chains through which the change propagates for those dependencies that you identified as the ones you include in your domain-specific and integration-related recommendations for ABB. Of course, if you have time, you can do this for all dependencies, but we encourage you to first make sure you derive insights for each domain and the integration view as described in Section 3 (ensuring you keep enough time for these main priority tasks).

Subsystem	Dependency	Used By	Strength
E1: Microcontroller (MCU-X)	Energy-Strong	E3:Existing test points (incl. TP3 - clock)	3
E1: Microcontroller (MCU-X)	Energy-Strong	E4: New test points (TP9, TP10)	3
E1: Microcontroller (MCU-X)	Energy-Weak	E2: Programming connector	1
E1: Microcontroller (MCU-X)	Energy-Weak	E6: PCB layout/pinout - DUT board, MCU area	1
E1: Microcontroller (MCU-X)	Info-Medium	E11: Technical documentation	2
E1: Microcontroller (MCU-X)	Info-Medium	E9: EOL test firmware	2
E1: Microcontroller (MCU-X)	Info-Strong	E5: DUT firmware	3
E1: Microcontroller (MCU-X)	Mechanical-Medium	E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer	2
E1: Microcontroller (MCU-X)	Mechanical-Strong	E6: PCB layout/pinout - DUT board, MCU area	3

Table 1: Microcontroller level 1 impact report

Subsystem	Dependency	Used By	Strength
E2: Programming connector	Energy-Weak	E7: EOL test bench adapter electrical layout	1
E2: Programming connector	Mechanical-Strong	E7: EOL test bench adapter electrical layout	3
E4: New test points (TP9, TP10)	Energy-Strong	E7: EOL test bench adapter electrical layout	3
E4: New test points (TP9, TP10)	Info-Medium	E10: FTM software	2
E5: DUT firmware	Info-Weak	E10: FTM software	1
E6: PCB layout/pinout - DUT board, MCU area	Energy-Weak	E7: EOL test bench adapter electrical layout	1
E6: PCB layout/pinout - DUT board, MCU area	Mechanical-Medium	E7: EOL test bench adapter electrical layout	2
E6: PCB layout/pinout - DUT board, MCU area	Mechanical-Strong	E1: Microcontroller (MCU-X)	3
E8: EOL test bench fixture (nest + pogo pins) – 3rd manufacturer	Mechanical-Medium	E1: Microcontroller (MCU-X)	2
E8: EOL test bench fixture (nest + pogo pins) – 3rd manufacturer	Mechanical-Strong	E7: EOL test bench adapter electrical layout	3
E9: EOL test firmware	Info-Medium	E10: FTM software	2

Table 2: Microcontroller level 2 impact report

Subsystem	Dependency	uses	Strength
E1: Microcontroller (MCU-X)	Manual	B1: SCM & Product Engineering	1
E1: Microcontroller (MCU-X)	Manual	B2: Product Owner	1
E1: Microcontroller (MCU-X)	Manual	B3: R&D – HW Designer	1
E1: Microcontroller (MCU-X)	Manual	B4: R&D – Electronic Layout	1
E1: Microcontroller (MCU-X)	Manual	B5: R&D – FW Designer	1
E1: Microcontroller (MCU-X)	Manual	B6: Test Engineering	1
E1: Microcontroller (MCU-X)	Manual	P10: INT:HW-SW integration	1
E1: Microcontroller (MCU-X)	Manual	P11: VAL::Internal Validation	1
E1: Microcontroller (MCU-X)	Manual	P12:FAT:Factory Acceptance Test	1
E1: Microcontroller (MCU-X)	Manual	P1: RS:Requirements/specifications receipt	1
E1: Microcontroller (MCU-X)	Manual	P2: DST:Test strategy definition	1
E1: Microcontroller (MCU-X)	Manual	P3: DE:Electrical design of test machine/fixture	1
E1: Microcontroller (MCU-X)	Manual	P7: SFW:Test firmware development	1
E1: Microcontroller (MCU-X)	Mechanical-Medium	E8: EOL test bench fixture (nest + pogo pins) - third-party manufacturer	2
E1: Microcontroller (MCU-X)	Mechanical-Strong	E6: PCB layout/pinout - DUT board, MCU area	3

Table 3: Microcontroller level 1 uses report

Subsystem	Dependency	uses	Strength
B6: Test Engineering	ORG-Moderate/formal	B9: FTM – Mechanical Fixture	2
B6: Test Engineering	ORG-Weak/Informal	B7: FTM – Firmware & Test Sequence	1
B6: Test Engineering	ORG-Weak/Informal	B8: FTM – Test Machine Hardware	1
E6: PCB layout/pinout - DUT board, MCU area	Energy-Weak	E2: Programming connector	1
E6: PCB layout/pinout - DUT board, MCU area	Info-Medium	E4: New test points (TP9, TP10)	2
E6: PCB layout/pinout - DUT board, MCU area	Manual	B8: FTM – Test Machine Hardware	1
E6: PCB layout/pinout - DUT board, MCU area	Manual	B9: FTM – Mechanical Fixture	1
E6: PCB layout/pinout - DUT board, MCU area	Manual	P4: DM:Mechanical fixture design	1
E6: PCB layout/pinout - DUT board, MCU area	Manual	P5: AC:Componet procurement	1
E6: PCB layout/pinout - DUT board, MCU area	Manual	P6: RM:Test machine/fixture manufacturing	1
E6: PCB layout/pinout - DUT board, MCU area	Manual	P9: ASM: Assembly	1
E6: PCB layout/pinout - DUT board, MCU area	Mechanical-Medium	E2: Programming connector	2
E6: PCB layout/pinout - DUT board, MCU area	Mechanical-Medium	E7: EOL test bench adapter electrical layout	2
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Energy-Medium	E3:Existing test points (incl. TP3 - clock)	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Energy-Weak	E2: Programming connector	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Energy-Weak	E4: New test points (TP9, TP10)	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Energy-Weak	E7: EOL test bench adapter electrical layout	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Manual	B8: FTM – Test Machine Hardware	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Manual	B9: FTM – Mechanical Fixture	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Manual	P4: DM:Mechanical fixture design	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Manual	P5: AC:Componet procurement	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Manual	P6: RM:Test machine/fixture manufacturing	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Manual	P9: ASM: Assembly	1
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Mechanical-Strong	E2: Programming connector	3
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Mechanical-Strong	E4: New test points (TP9, TP10)	3
E8: EOL test bench fixture (nest + pogo pins) - 3rd manufacturer	Mechanical-Strong	E7: EOL test bench adapter electrical layout	3
P10: INT:HW-SW integration	Manual	B7: FTM – Firmware & Test Sequence	1
P10: INT:HW-SW integration	Manual	B8: FTM – Test Machine Hardware	1
P10: INT:HW-SW integration	Manual	B9: FTM – Mechanical Fixture	1
P10: INT:HW-SW integration	P-Structural	P8: SSQ:Test sequence development	3
P10: INT:HW-SW integration	P-Structural	P9: ASM: Assembly	3
P11: VAL::Internal Validation	Manual	B7: FTM – Firmware & Test Sequence	1
P11: VAL::Internal Validation	Manual	B8: FTM – Test Machine Hardware	1
P11: VAL::Internal Validation	Manual	B9: FTM – Mechanical Fixture	1
P12:FAT:Factory Acceptance Test	Manual	B7: FTM – Firmware & Test Sequence	1
P12:FAT:Factory Acceptance Test	Manual	B8: FTM – Test Machine Hardware	1
P12:FAT:Factory Acceptance Test	Manual	B9: FTM – Mechanical Fixture	1
P3: DE:Electrical design of test machine/fixture	Feedback	P4: DM:Mechanical fixture design	3
P3: DE:Electrical design of test machine/fixture	Manual	B8: FTM – Test Machine Hardware	1
P7: SFW:Test firmware development	Manual	B7: FTM – Firmware & Test Sequence	1

Table 4: Microcontroller level 2 uses report

7 Guideline

1. Familiarize yourself with the data provided and try to understand the three domains and the underlying dependencies. Identify potentially missing descriptions.
2. Use the provided pre-analyzed models to derive possible changes in each domain and in the "integration view" of all three domains. You could, for example, consider for your discussions:
    - Identifying strong dependencies: could they be eliminated?
    - Identifying feedback loops: could the process be re-arranged to prevent/reduce them?
    - Identifying activities that can run in parallel
    - Identifying unnecessary handovers
    - Identifying opportunities to standardize or modularize the FTM (product domain)
    - Redefining responsibilities and interfaces
    - Proposing a new Product–Process–Organization architecture
3. We suggest to approximately distribute your time as follows:
    - 15 min reading & understanding
    - 20 min on each domain (60 min total)
    - 45 min lunch break
    - 30 min lab tour (your group will be called separately)
    - 30 min integration view
    - 30 min presentation preparation
4. In addition to the already presented models, we will provide you with the original dataset that ABB has provided us with. While our target was to condense and pre-structure the data for you with this task document, we understand that some of you might want to also view the original dataset. However, we want to emphasize that the task is designed so you do not necessarily have to do this. We therefore recommend to only review this dataset by the time you have developed a clear understanding of the systems and your suggested changes for additional insights.
5. Remember to use the option of consulting one of our Lattix experts where needed.
6. Answer all "what we ask of you" aspects from Section 3 (page 2).

8 Required tools

This year's ISW challenge is designed to not require any specific software. You will just need a **pdf reader** for this document and **Excel** (only if you want to look into the additional dataset).

9 Provided data

On the ISW website, you will find the following provided data:

- Digital file of this challenge narrative
- Additional background excel file (not required to solve the task)

All data is password-secured. The password is given in an email sent to every participant. Further, you have access to the "live" Lattix models at the ISW through our Lattix experts.